MITEL
SEMICONDUCTOR

NWK939

10/100 Base-TX Symbol Transeiver

Advance Information

DS4733 - 2.2 January 1998

The NWK939 is a CMOS Fast Ethernet Transceiver with integrated clock and data recovery for combined 10BASE-T and 100BASE-TX applications. The device connects through a 5 bit symbol interface directly with the NWK960 and similar controllers that incorporate the PCS function such as the DEC21143. The NWK939 incorporates on-chip filtering and pulse shaping to allow use of common 1:1 magnetics (isolation transformers) for both 10 Mb/s and 100 Mb/s modes.

FEATURES

- 10BASE-T and 100BASE-TX switchable
- IEEE-802.3 compatible
- Connects with NWK960 for complete 10/100 NIC solution
- Single 1:1 magnetics module for both 10BASE-T and 100BASE-TX
- Industry standard Symbol Interface
- Supports half and full-duplex operation
- Low latency
- Integrated diagnostic loopback
- Low power mode
- Operates with crystal oscillator or external clock source
- Integrated filters and pulse shaping
- Quantized Feedback circuitry to correct Base Line Wander
- Integrated clock recovery and clock synthesis
- Integrated adaptive equalizer
- Full support for auto-negotiation signalling
- Internal loop filter components
- Low external component count

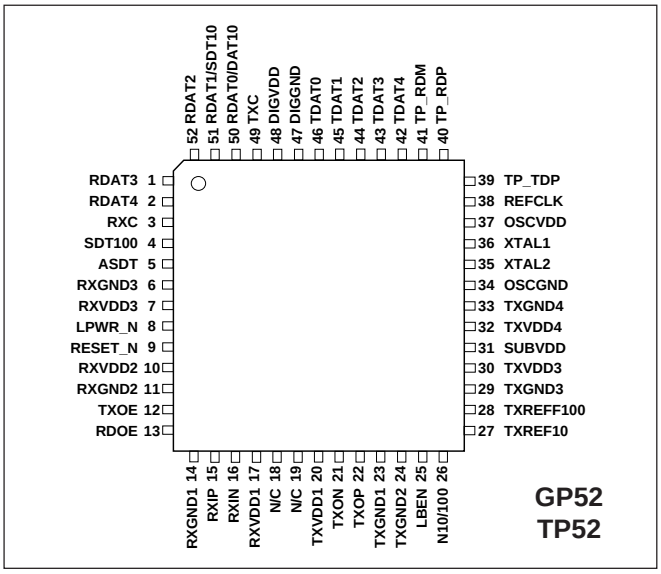


Fig.1 Pin connections - top view

- Low power CMOS technology
- Single +5V supply
- 52 Pin PQFP package
- Also available in Thin PQFP package

ORDERING INFORMATION

NWK939C/CG/GH1N
NWK939/CG/TP1N thin quad

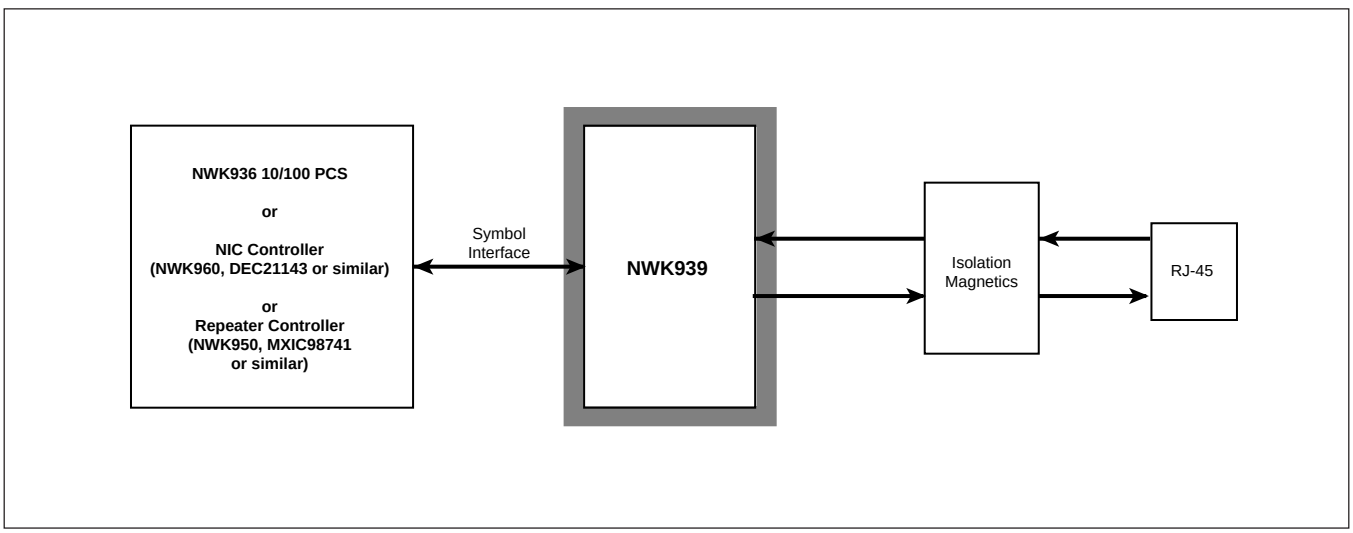


Fig.2 System block diagram

OVERVIEW

The NWK939 is a mixed-signal CMOS 10/100Mb/s transceiver which integrates all of the signal processing components of the dual speed Ethernet Physical Layer. It is designed for compliance with IEEE802.3 Standards and directly interfaces to a variety of Network Interface Card and Repeater controller devices through the industry standard symbol interface. The NWK939 employs robust design techniques to provide a very low bit-error rate and automatic recovery from fault conditions.

Compliance to Standards

The NWK939 is designed for compliance with the IEEE 802.3 Standard, Clauses 14, 24 & 25, henceforth referred to as 802.3. The 802.3 PMD sub-layer for 100BASE-TX is derived from the FDDI TP-PMD Standard, henceforth referred to as TP-PMD.

Compatibility With Other Devices

For Network Interface Card applications the NWK939 is designed to operate with controllers such as the NWK960 and the DEC21143, connecting via the symbol interface.

For 100BASE-TX repeater applications the NWK939 is designed to operate with controllers such as the NWK950 and MXIC98741, also connecting via the symbol interface.

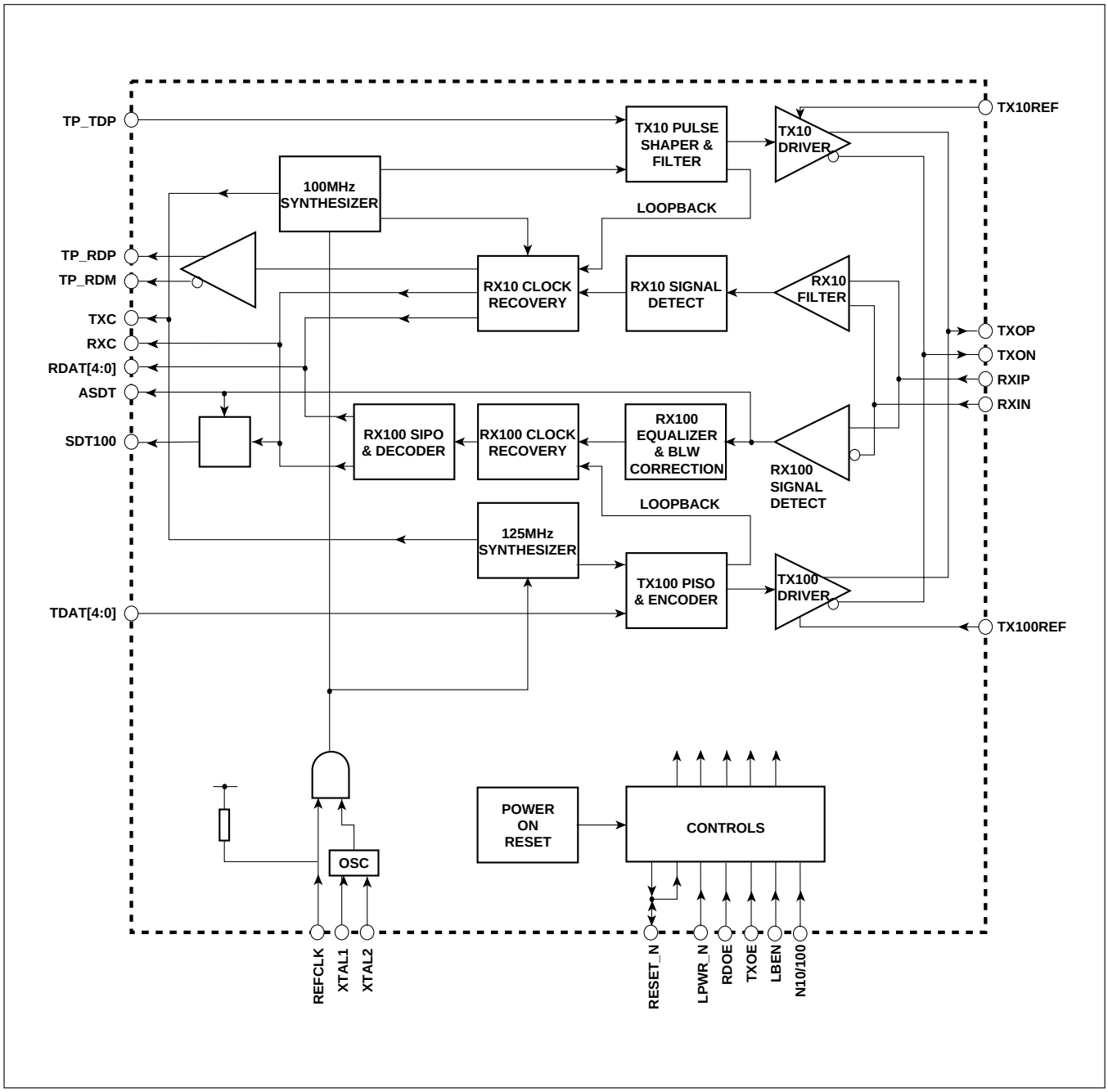


Fig.3 NWK939 block diagram

FUNCTIONAL DESCRIPTION

The NWK939 has three operating modes: 10BASE-T mode, 100BASE-TX mode and LOW-POWER mode. The modes are selected by the N10/100 and LPWR_N pins.The Control block is designed to manage these modes by starting and stopping the two transceivers in a well-controlled manner such that no spurious signals are output on either the symbol or twisted-pair interfaces. Furthermore, it continuously monitors the behaviour of the transceivers and takes corrective action if a fault is detected.

25MHz REFERENCE CLOCK

The NWK939 requires a 25MHz +/-100ppm timing reference for 802.3 compliant operation. This may be supplied either from the integrated oscillator or from an external source. When the integrated oscillator is used, a suitable crystal must be connected across the XTAL1 & XTAL2 pins (see “External Components”). When an external source is used, it must be input to the REFCLK pin and XTAL1 must be tied high. XTAL2 must be unconnected.

10BASE-T OPERATION

In 10BASE-T mode Manchester encoded serial data is loaded from the TP_TDP input, processed through the TX10 Path and output on the TXOP/TXON differential output for transmission through 1:1 magnetics and onto the twisted-pair.

The incoming signal received from the magnetics into the RXIP/RXIN differential input is processed through the RX10 Path. Received data is output serially on 2 interfaces. The DAT10 & SDT10 signals form a Mitel Semiconductor-specific interface for connection to the NWK936 PCS device. For NIC controllers that have in-built 10BASE-T receivers, the received signal is also provided on the TP_RDP/TP_RDM differential output. The TX10 & RX10 paths are disabled when the device is not in 10BASE-T mode.

100MHz Synthesizer

This synthesizer employs a delay-locked loop (DLL) to generate a 100MHz timing reference from the 25MHz reference clock. This 100MHz reference is used by the 10BASE-T transmit and receive functions and is divided by 5 to provide a 20MHz data strobe on TXC. The synthesizer is disabled when not in 10BASE-T mode.

TX10 Pulse Shaper & Filter

This block loads Link Pulses and Manchester encoded serial data from the TP_TDP input on the falling edge of TXC. This input may be connected directly to the TP_TDP output of the DEC21143 and similar NIC controllers. The Pulse Shaper & Filter employs a digital finite impulse response filter (FIR) to pre-compensate for line distortion and to remove high frequency components in accordance with the 802.3 Standard. The Pulse Shaper & Filter is disabled when not in 10BASE-T mode.

TX10 Driver

The TX10 Driver operates with 1:1 magnetics to provide impedance matching and amplification of the signal in accordance with the 802.3 specifications. The transmit current is governed by the current through the TXREF10 pin, which must be grounded through a resistor as described in “External Components”.

TX10 Latency

When connected to appropriate magnetics the latency through the TX10 path is less than 1BT (100ns) for data transmissions. This timing is measured from the falling edge of TXC to the output of the transmit magnetics. The TX10 path will not transmit the first two Manchester encoded bits of a data transmission, as permitted by the 802.3 Standard.

RX10 Filter & RX10 Signal Detect

These blocks work in unison to remove noise and to block signals that do not achieve the voltage levels specified in 802.3. Signals that do not achieve the required level are not sampled in the Clock Recovery block and are not passed to the DAT10/ SDT10 and TP_RDP/TP_RDM outputs.

RX10 Clock Recovery

The RX10 Clock Recovery employs a digital delay line controlled by the 100MHz Synthesizer DLL to derive a sampling clock from the incoming signal. The recovered clock runs at twice the data rate (nominally 20MHz). When a signal is received from the Signal Detect block, SDT10 is asserted and falling RXC is used to strobe Link Pulses and Manchester encoded serial data out on DAT10 and TP_RDP/TP_RDM. When no signal is being received, SDT10 is deasserted, RXC is driven from the 20MHz transmit clock, DAT10 is held low and TP_RDP/TP_RDM is driven to the zero state (see “DC Electrical Characteristics”).

RX10 Latency

When connected to appropriate magnetics the latency through the RX10 path is less than 1BT (100ns). This timing is measured from the input of the receive magnetics to the falling edge of RXC. The RX10 path may ignore up to three Manchester encoded bits at the start of data reception (802.3 allows up to 5 bits) and the first bit forwarded to TP_RDP/TP_RDM may have timing violations (802.3 allows 1 bit).

100BASE-TX OPERATION

In 100BASE-TX mode 5-bit NRZ symbols are loaded from the TDAT bus, processed through the TX100 Path and output on the TXOP/TXON differential output for transmission through the 1:1 magnetics and onto the twisted-pair.

The incoming signal received from the magnetics into the RXIP/RXIN differential input is processed through the RX100 Path and output in 5-bit parallel NRZ form on the RDAT bus. The TX100 path is disabled when not in 100BASE-TX mode and, with the exception of the RX100 Signal Detect, the RX100 Receive Path is disabled when not in 100BASE-TX mode.

125MHz Synthesizer

This synthesizer employs a phase-locked loop (PLL) to generate a 125MHz timing reference from the 25MHz reference clock. This 125MHz reference is used by the 100BASE-TX transmit function and is divided by 5 to provide a 25MHz data strobe on TXC. TXC is frequency and phase locked to the 25MHz reference with a small phase offset. The synthesizer is disabled when not in 100BASE-TX mode.

TX100 PISO & Encoder

The TX100 PISO & Encoder loads NRZ-coded symbols from TDAT on the rising edge of TXC, and converts them to serial MLT3 for outputting to the TX100 Driver. The TDAT[4] bit is output first. The PISO & Encoder do not operate until the 125MHz Synthesizer is locked to the 25MHz reference. This avoids transmission of spurious signals onto the twisted-pair.

TX100 Driver

The TX100 Driver outputs the differential signal onto the TXOP and TXON pins. It operates with 1:1 magnetics to provide impedance matching and amplification of the signal in accordance with the 802.3 specifications. The transmit current is governed by the current through the TXREF100 pin, which must be grounded through a resistor as described in “External Components”. The TX100 driver is disabled in 10BASE-T mode and when LBEN is active.

TX100 Latency

When connected to appropriate magnetics the typical latency through the TX100 path is 1.2BT (12ns). This timing is measured from the rising edge of TXC to the output of the transmit magnetics.

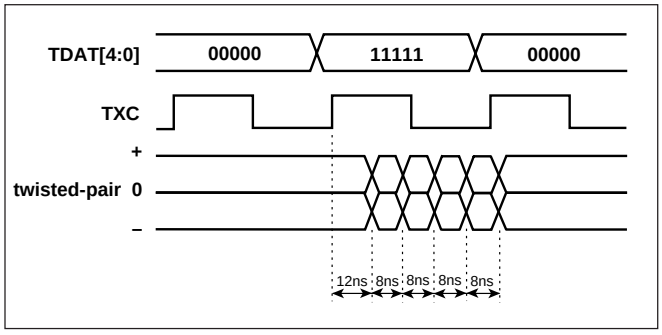


Fig.4 100BASE-TX transmit latency

RX100 Signal Detect

The RX100 Signal Detect continuously monitors the level on the RXIP/N differential input. ASDT (Asynchronous Signal Detect) will be asserted high whenever the signal amplitude exceeds the minimum that can be handled by the RX100 Equalizer. RX100 Signal Detect does not discriminate between signal types, therefore ASDT will be asserted for 10BASE-T signals and Link Pulses as well as for100BASE-TX signals. RX100 Signal Detect is continuously active in all 3 operating modes, therefore ASDT may be used to externally generate a wake-up signal when the device is in LOW-POWER mode.

RX100 Signal Detect also generates SDT100 which is a synchronous version of ASDT. SDT100 is synchronous to RXC rising and operates in both 10BASE-T mode and 100BASE-TX mode. In LOW-POWER mode RXC is stopped and SDT100 is driven low.

RX100 Equalizer & Base-line Wander Correction

The RX100 Equalizer compensates for the signal attenuation and distortion resulting from transmission down the cable and through the isolation transformers. The Equalizer is self-adjusting and is designed to restore signals received from up to 10dB cable attenuation. The Equalizer is inactive when ASDT is deasserted. When ASDT is asserted high, the Equalizer adjusts to the incoming signal within 1ms. Thereafter, the Equalizer will continuously adjust to small variations in signal level without corrupting the received data.

The 100BASE-TX MLT3 code contains significant low frequency components which are not passed through the isolation transformers and cannot be restored by an adaptive equalizer. This leads to a phenomenon known as base-line wander which will cause an unacceptable increase in error rate if not corrected. The NWK939 employs a quantized feedback technique to restore the low frequency components and thus maintain a very low error rate even when receiving signals such as the “killer packet” described in the TP_PMD spec.

RX100 Clock Recovery

The RX100 Clock Recovery circuit uses a Phase-Locked Loop (PLL) to derive a sampling clock from the incoming signal. The recovered clock runs at the symbol bit rate rate (nominally 125MHz) and is used to clock the MLT3 decoder and the Serial to Parallel converter (SIPO). The recovered clock is divided by 5 to generate the receive clock (RXC) which is used to strobe received data across the symbol interface. When ASDT is deasserted in 100BASE-TX mode, the PLL is locked to the reference clock and runs at 125MHz. This ensures that RXC runs continuously at 25MHz in 100BASE-TX mode. When ASDT is asserted high, the Clock Recovery PLL remains locked to the reference until the equalizer has adjusted, then it requires up to 1ms to phase lock to the incoming signal. No data is passed to the symbol interface until lock is established.

RX100 SIPO & Decoder

The RX100 SIPO & Decoder converts the received signal from serial MLT3 to 5-bit parallel NRZ which is output on RDAT. The NWK939 does not align received symbols to the RDAT bus. When ASDT is deasserted, RDAT is driven low. RDAT will continue to be driven low until ASDT is asserted, the Equalizer has adjusted, and the Clock Recovery is phase locked to the incoming signal. This ensures that no invalid data is passed to the higher layers.

RX100 Latency

The typical latency through the RX100 Receive Path is 6.4BT (64ns). This timing is measured from the start of a bit seen on the twisted-pair medium to the RXC falling edge that outputs that bit to the RDAT bus. The bit may appear in any position on RDAT, and therefore the latency varies as follows:

twisted-pair -> RDAT[4] = 64ns
twisted-pair -> RDAT[3] = 56ns
twisted-pair -> RDAT[2] = 48ns
twisted-pair -> RDAT[1] = 40ns
twisted-pair -> RDAT[0] = 32ns

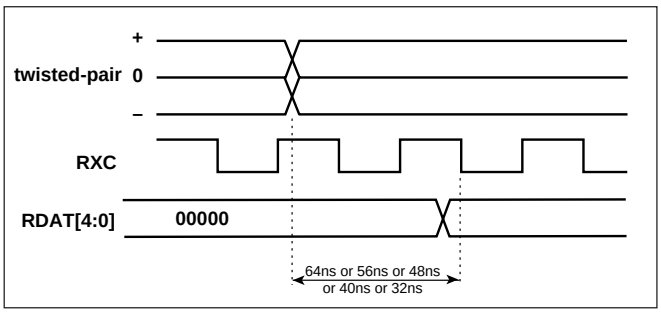


Fig.5 100BASE-TX receive latency

LOW-POWER OPERATION

In LOW-POWER mode the 10BASE-T and 100BASE-TX transceivers are disabled. This mode is intended to conserve power when the network connection is not required.

The synthesizers and all TX10 & TX100 functions are disabled and the TXOP/TXON output is undriven.

The oscillator continues to run and the 25MHz reference will be driven out onto TXC if RDOE is asserted. This facility is provided for interfacing to the DEC21143 where a continuous clock is required.

All RX10 & RX100 functions except RX100 Signal Detect are disabled. RX100 Signal Detect continues to monitor the RXIP/RXIN input and to drive ASDT accordingly. ASDT may therefore be used to externally generate a wake-up signal.

The RXC clock is stopped in LOW-POWER mode and the RDAT & SDT100 outputs are held low.

CONTROL SIGNALS

Initialization, mode selection and other options are governed by the control inputs as described in the following paragraphs.

Initialization (RESET_N)

The NWK939 incorporates a power-on-reset circuit for self-initialization on power-up. During initialization the open-drain RESET_N pin is driven low and all data outputs are disabled to prevent spurious outputs to the twisted-pair and to the symbol interface. RESET_N will remain low until either the 10BASE-T or 100BASE-TX transceiver has been correctly initialized. The NWK939 will then release RESET_N allowing the external pull-up to pull the pin high. Data transmission and reception will not commence until RESET_N is high. This allows the user to extend the inactive period by externally holding RESET_N low. It will not normally be necessary for the user to drive RESET_N because the NWK939 is designed to automatically recover from fault conditions, however if required, the user may initialize the device by pulsing RESET_N low.

Note 1: Holding RESET_N low will not hold the device in a static, low power state. It will initialize the selected transceiver and start the appropriate clocks. For power saving use the LPWR_N pin.

Note 2: The NWK936 PCS device is initialized by connecting its RESET_N input to the NWK939 pin.

Note 3: If the NWK939 is powered-up with LPWR_N low, then the device will immediately enter LOW-POWER mode and RESET_N will be held low until LPWR_N is deasserted and one of the transceivers is started up.

Mode Selection (LPWR_N & N10/100)

LOW-POWER mode can be selected at any time by asserting LPWR_N low. When LPWR_N is inactive, 10BASE-T mode is selected by pulling N10/100 low, 100BASE-TX mode is selected by pulling N10/100 high. During mode changes the TXC & RXC clocks will continue to run but there will be no data transfers until the appropriate transceiver has been started up.

Diagnostic Loopback (LBEN)

Diagnostic loopback may be selected at any time by asserting LBEN high. In 10BASE-T mode transmission to the TXOP/TXON output will be stopped and the RX10 Clock Recovery will receive input from the TX10 transmit path rather than from the RXIP/RXIN inputs. In 100BASE-TX mode transmission to the TXOP/TXON output will be stopped, the RX100 Clock Recovery will receive input from the TX100 transmit path and SDT100 will be forced high.

Transmitter Output Enable (TXOE)

The TX10 Driver & TX100 Driver may be disabled by driving TXOE low. This control signal is provided for compatibility with earlier Mitel Semiconductor transceivers. It provides modest power savings and can be used to reduce EMI generation from unconnected twisted-pair ports, but is superseded on the NWK939 by the LOW-POWER mode.

Receive Data Output Enable (RDOE)

This signal must be pulled high when interfacing to DEC21143 and similar NIC controllers. RDOE enables the TP_RDP/TP_RDM output and also keeps TXC running in LOW_POWER mode. In 100Mb/s-only applications, or when interfacing to the NWK936, noise and power savings may be achieved by setting RDOE low.

INTERFACE DESCRIPTIONS

10BASE-T Transmit Data (TP_TDP)

In 10BASE-T mode Link Pulses and Manchester encoded serial data are loaded from the TP_TDP input for transmission on the twisted-pair. TP_TDP is sampled on the falling edge of TXC. The TP_TDP input is designed to be driven from either the DEC21143 TP_TDP output or the NWK936 TP_TDP output.

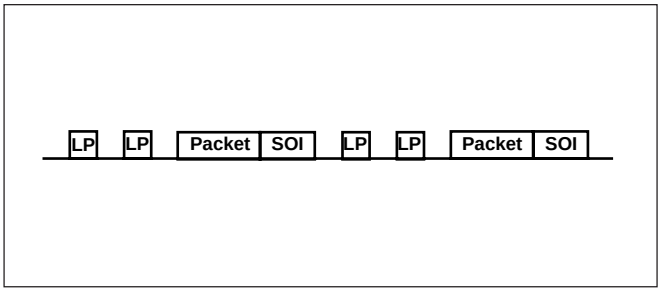


Fig.6 Signals on TP_TDP

10BASE-T data transmissions consist of Manchester encoded data packets separated by an idle pattern (see Fig.6). The idle pattern comprises a Start-of-Idle (SOI) pulse which is appended to the end of each packet, and Link Pulses at 8 to 24ms intervals. During 802.3 Auto-negotiation a faster burst of Link Pulses is transmitted.

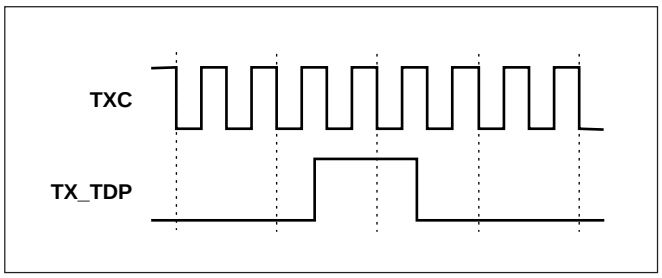


Fig.7 Link pulse on TP_TDP

When no transmission is required, the TP_TDP input must be held low. To initiate Link Pulse transmission, TP_TDP should be driven high for 2 cycles of TXC (see Fig. 7). The NWK939 requires that the interval between Link Pulses be greater than 10 cycles of TXC (500ns).

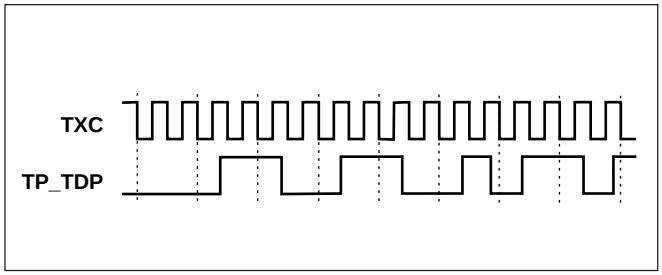


Fig.8 Packet on TP_TDP

For data packet transmission the Manchester encoded data must be presented to the TP_TDP input (see Fig. 8).

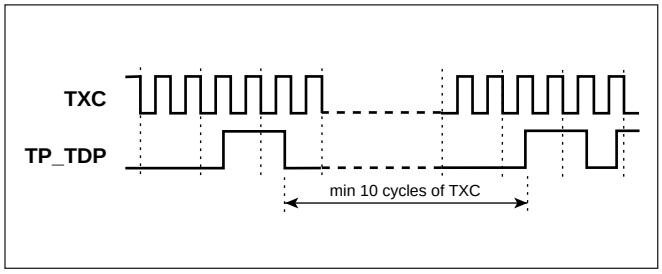


Fig.9 Interval between link pulse and packet

The interval between a Link Pulse and the first logic 1 in the packet signal should be greater than 10 cycles of TXC (see Fig. 9). If the interval is less than 10 cycles then the first bit of the packet transmission may be corrupted, but the corruption will be within that allowed by 802.3.

The SOI pulse will be transmitted if the TP_TDP input is held high for 6 cycles of TXC at the end of the data packet. If the last data bit transmitted was a logic 1 then the latter half of this bit will merge with the SOI pulse such that TP_TDP is high for 7 cycles of TXC (see Fig.10).

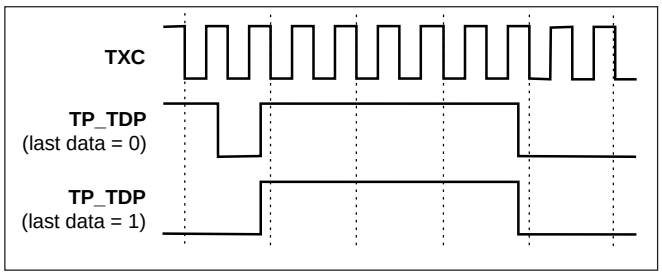


Fig.10 Start-of-Idle on TP_TDP

The TP_TDP input is ignored when the device is not in 10BASE_T mode.

10BASE_T Receive Data (TP_RDP/TP_RDM)

This serial interface is for passing received signals to the DEC21143 and similar controllers. TP_RDP/TP_RDM is equivalent to the signal received on RXIP/RXIN after filtering, jitter reduction and suppression of low level signals. The TP_RDP/TP_RDM output is disabled when RDOE is deasserted and when the device is not in 10BASE-T mode.

10BASE_T Receive Data (DAT10 & SDT10)

This serial interface is for passing received signals to the NWK936 PCS device. In 10BASE-T mode DAT10 & SDT10 are multiplexed onto RDAT[0:1] and the remaining bits of RDAT are held low. The DAT10 & SDT10 outputs are synchronous to RXC falling and are intended to be sampled by the NWK936 on RXC rising. When no signal is being received from the twisted-pair both DAT10 & SDT10 are held low.

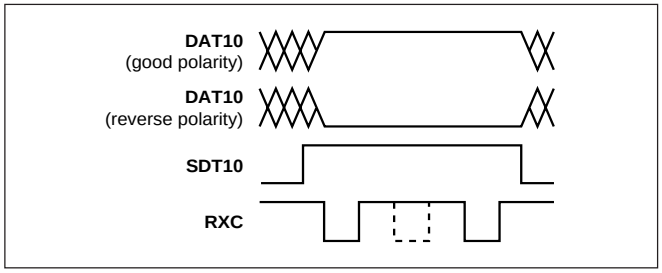


Fig.11 Link pulse on DAT10 & SDT10

When a Link Pulse is received SDT10 will be asserted high for 2 or 3 cycles of RXC (see Fig. 11). If the Link Pulse has the correct polarity then DAT10 will also be asserted high. If the polarity is reversed due to a twisted-pair wiring fault, then DAT10 will remain low during reception of the Link Pulse. The NWK936 will check and correct for polarity reversal. Packet data and Start-of-Idle (SOI) pulse reception are illustrated in Figs. 12 & 13.

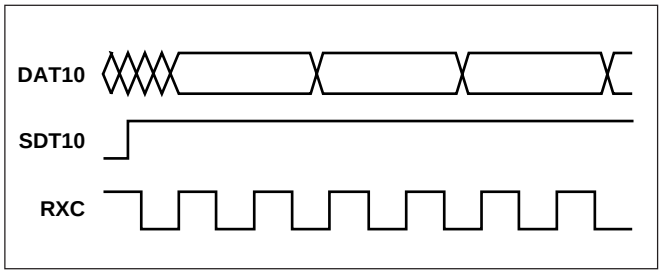


Fig.12 Start of packet on DAT10 & SDT10

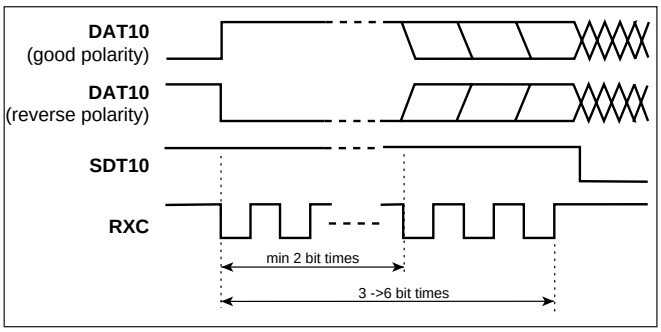


Fig.13 Start-of-Idle on DAT10 & SDT10

100BASE-TX Transmit Data (TDAT)

In 100BASE-TX mode symbol data is loaded from TDAT on TXC rising. Symbol data is defined as data which is 4B/5B encoded and scrambled. The user may present data either on TXC or on REFCLK (if the integrated oscillator is not being used). TXC & REFCLK are frequency and phase locked with a small phase error. TDAT timing is quoted with respect to both clocks, see “AC Electrical Characteristics”. TDAT is ignored when the device is not in 100BASE-TX mode.

100BASE-TX Receive Data (RDAT)

In 100BASE-TX mode received symbols are output on RDAT on RXC falling. The data is 5-bit parallel but symbols are not aligned to the bus.

Transmit Clock (TXC)

In 10BASE-T mode TXC is a continuous 20MHz clock. In 100BASE-TX mode TXC is a continuous 25MHz clock, frequency & phase locked to the 25MHz reference. In LOW-POWER mode TXC is driven from the 25MHz reference if RDOE is asserted, otherwise it is held low. On power-up, or following an external reset, TXC will be held low until the appropriate clock source is available and within specification. TXC starts up cleanly, i.e. with no short pulses or spikes. When the operating mode is changed, TXC continues to be driven from the old source until the new source is available and within specification. At changeover there will be no spikes, but TXC will have extended timing for one cycle only, see “AC Electrical Characteristics” for details. These specifications for start up and changeover ensure that higher layer devices can safely use TXC. In particular, it can be used as the source of the MII TX_CLK. When working with the DEC21143 TXC should be used to drive the SYM_TCLK & XTAL1 inputs.

Receive Clock (RXC)

In 10BASE-T mode RXC is a continuous clock. During signal reception it is recovered from the incoming signal and runs nominally at 20MHz. When no signal is being received it is driven from the 20MHz transmit clock. At the start of data reception RXC must synchronise to the incoming signal, during this time RXC conforms to the “during synchronization” timing indicated in “AC Electrical Characteristics”.

In 100BASE-TX mode RXC is a continuous clock recovered from the incoming signal and running nominally at 25MHz. When there is no incoming signal the clock recovery PLL locks to the 25MHz reference. In LOW-POWER mode RXC is held low. On power-up, or following an external reset, RXC will be held low until the appropriate clock source is available and within specification. RXC starts up cleanly, i.e. with no short pulses or spikes. When the operating mode is changed, RXC continues to be driven from the old source until the new source is available and within specification. At changeover there will be no spikes, but RXC will have extended timing for one cycle only, see “AC Electrical Characteristics” for details. These specifications for start up and changeover ensure that higher layer devices can safely use RXC. In particular, it can be used as the source of the MII RX_CLK. When working with the DEC21143 RXC should be used to drive the SYM_RCLK input.

Signal Detect (ASDT & SDT100)

ASDT (Asynchronous Signal Detect) will be asserted high whenever the signal amplitude exceeds the minimum that can be handled by the RX100 Equalizer. ASDT does not discriminate between signal types, and therefore will be asserted for 10BASE-T signals and Link Pulses as well as for 100BASE-TX signals. ASDT is available in all 3 operating modes, therefore may be used to externally generate a wake-up signal when the device is in LOW-POWER mode.

SDT100 is a synchronized and filtered version of ASDT, intended for connection to controllers such as the DEC21143. SDT100 is synchronous to RXC rising and pulses shorter than 30μs are filtered out. In 10BASE-T mode and 100BASE-TX mode, SDT100 will respond to valid 100BASE-TX signals and 10BASE-T packets but will not respond to 10BASE-T Link Pulses. In LOW-POWER mode RXC is stopped and SDT100 is driven low.

PIN DESCRIPTIONS

Pin Name	Pin Type	Pin Number	Pin Description
SYMBOL Interface			
RXC	digital output	3	**Receive Clock.** Recovered from the incoming signal. Derived from the reference clock when no incoming signal. Runs at 25MHz nominal in 100BASE-TX mode, 20MHz nominal in 10BASE-T mode, and is held low in LOW-POWER mode.
SDT100	digital output	4	**100BASE-TX Signal Detect.** Active high, synchronous to RXC rising. Indicates the incoming signal exceeds 100BASE-TX thresholds. Operates in both 100BASE-TX & 10BASE-T modes. Held low in LOW-POWER mode. (Note: this signal responds to both 100BASE-TX & 10BASE-T signals.)
ASDT	digital output	5	**Asynchronous Signal Detect.** Active high, independent of all clocks. Indicates that the incoming signal exceeds 100BASE-TX thresholds. Operates in 100BASE-TX, 10BASE-T & LOW-POWER modes. (Note: this signal responds to both 100BASE-TX & 10BASE-T signals.)
TDAT4 TDAT3 TDAT2 TDAT1 TDAT0	digital inputs no pull-up	42 43 44 45 46	**100BASE-TX Transmit Data.** In 100BASE-TX mode, transmit symbols (i.e. encoded & scrambled data) are loaded on TXC rising. TDAT4 is transmitted first. These inputs are ignored in 10BASE-T & LOW-POWER modes.
TXC	digital output	49	**Transmit Clock.** Runs at 25MHz in 100BASE-TX mode and 20MHz in 10BASE-T mode. In LOW-POWER mode TXC runs at 25MHz if RDOE=1, or is held low if RDOE=0.
RDAT0/DAT10 RDAT1/SDT10 RDAT2 RDAT3 RDAT4	digital outputs	50 51 52 1 2	**Receive Data.** Synchronous to RXC falling. In 100BASE-TX mode received symbols (i.e. encoded & scrambled data) are output on RDAT[4:0]. RDAT4 is the first bit received, symbols are not aligned to the bus. In 10BASE-T mode serial Manchester encoded receive data is output on DAT10, and SDT10 indicates the incoming signal exceeds 10BASE-T thresholds. In LOW-POWER mode RDAT[4:0] is held low.
Network Interface			
RXIP RXIN	differential analog input	15 16	**Receive Input.** Input from the magnetics for both 100BASE-TX and 10BASE-T reception.
TXOP TXON	differential analog output	22 21	**Transmit Output.** Output to the magnetics for both 100BASE-TX and 10BASE-T transmission. High impedance in LOW-POWER mode and when TXOE=0.
TXOE	digital input no pull-up	12	**Transmit Output Enable.** Active high. Enables the TXOP/TXON output.
10BASE-T Interface			
TP_RDM TP_RDP	differential analog output	41 40	**10BASE-T Receive Signal.** In 10BASE-T mode this is a filtered and retimed copy of the twisted-pair receive signal. Held in the zero state (TP-RDP = TP-RDM) in 100BASE-TX and LOW-POWER modes. High impedance when RDOE=0.
RDOE	digital input no pull-up	13	**Receive differential output enable.** Active high. Enables the TP-RDP/ TP-RDM output.
TP_TDP	digital input no pull-up	39	**10BaseT Transmit Data.** In 10BASE-T mode, serial Manchester encoded data is loaded on TXC falling. This input is ignored in 100BASE-TX & LOW-POWER modes.

PIN DESCRIPTIONS CONT.

Pin Name	Pin Type	Pin Number	Pin Description
Control Pins			
LBEN	digital input no pull-up	25	**Loopback Enable.** Active high. Enables internal loopback for diagnostic purposes in both 100BASE-TX & 10BASE-T modes. Suppresses transmission on TXOP/TXON.
N10/100	digital input no pull-up	26	**10BASE-T/100BASE-TX Select.** Low selects 10BASE-T mode, high selects 100BASE-TX mode.
RESET_N	open drain digital output with digital input,no pull up	9	**Reset.** Active low, bidirectional. Driven low by the NWK939 during initialisation. May be driven low from an external source to retrigger or extend initialisation.
LPWR_N	digital input no pull-up	8	**LOW-POWER Mode Select.** Active low.
TXREF10	analog	27	**10BASE-T Transmitter Reference.** Sets the 10BASE-T transmitter current. Connect to ground through external resistor.
TXREF100	analog	28	**100BASE-TX Transmitter Reference.** Sets the 100BASE-TX transmitter current. Connect to ground through external resistor.
Clocks			
REFCLK	digital input with pull-up	38	**25MHz Reference.** Drive from external 25MHz source when the on-chip oscillator is not used. Connect to OSCVDD when on-chip oscillator is used.
XTAL1	analog	36	**25MHz crystal input.** Connect to OSCVDD when the on-chip oscillator is not used.
XTAL2	analog	35	**25MHz crystal input.** Leave unconnected when the on-chip oscillator is not used.
Power			
DIGGND	ground	47	**Digital ground**
DIGVDD	power	48	**Digital power**
RXGND	ground	6,11,14	**Receive ground**
RXVDD	power	7,10,17	**Receive power**
TXGND	ground	23,24,29,33	**Transmitter ground**
TXVDD	power	20,30,32	**Transmitter power**
OSCGND	ground	34	**Oscillator ground**
OSCVDD	power	37	**Oscillator power**
SUBVDD	power	31	**Substrate power**
No Connects			
-	-	18	**do not connect to this pin**
-	-	19	**do not connect to this pin**

ABSOLUTE MAXIMUM RATINGS

Exceeding the absolute maximum ratings may cause permanent damage to the device. Extended exposure at the maximum ratings will affect device reliability.

Supply voltage (V_{DD})	–0.5 to +7V
Input voltage	–0.5 to V_{DD}+0.5V
Output voltage	–0.5 to V_{DD}+0.5V
Static discharge voltage	4kV HBM
Storage temperature (T_A)	-40 to +125°C

RECOMMENDED OPERATING CONDITIONS

Neither performance nor reliability are guaranteed outside these limits. Extended operation above these limits may affect device reliability.

Supply voltage (V_{DD})	+5V ±5%
Input voltage	0 to V_{DD}
Output voltage	0 to V_{DD}
Current per pin	100mA
Ambient temperature (T_A)	0°C to +70°C

SUPPLY CURRENT

Recommended operating conditions apply except where stated.

Characteristic	Symbol	Value Min.	Typ.	Max.	Units	Conditions
10BASE-T mode, not transmitting	I_{DD}	-	105	115	mA	With external components as shown in Fig.14. Supply currents quoted here include currents through external components.
10BASE-T mode, transmitting	I_{DD}	-	178	190	mA	
100BASE-TX mode	I_{DD}	-	108	120	mA	
Low Power mode	I_{DD}	-	35	40	mA	

DC ELECTRICAL CHARACTERISTICS

Recommended operating conditions apply except where stated.

Characteristic	Symbol	Value Min.	Typ.	Max.	Units	Conditions
Digital input, no pull-up						
Input high voltage	V_{IH}	2	-	V_{DD}	V	
Input low voltage	V_{IL}	V_{SS}	-	0.8	V	
Hysteresis	V_H	0.3	-	-	V	
Input high current	I_{IH}	-	-	1	µA	
Input low current	I_{IL}	-	-	–1	µA	
Capacitance	C_I	-	-	8	pF	including package
Digital input, with pull-up						
Input high voltage	V_{IH}	2	-	V_{DD}	V	
Input low voltage	V_{IL}	V_{SS}	-	0.8	V	
Hysteresis	V_H	0.3	-	-	V	
Input high current	I_{IH}	-	-	1	µA	
Input low current	I_{IL}	–17	-	–130	µA	
Capacitance	C_I	-	-	8	pF	including package
Digital output						
Output high voltage	V_{OH}	4	-	V_{DD}	V	I_{OH} = –6mA
Output low voltage	V_{OL}	V_{SS}	-	0.4	V	I_{OL} = 6mA
Rise time	t_R	-	-	4	ns	0.4V to 2.4V into 20pF
Fall time	t_F	-	-	3	ns	2.4V to 0.4V into 20pF
Capacitance	C_O	-	-	8	pF	including package
Open drain digital output						
Output low voltage	V_{OL}	V_{SS}	-	0.4	V	I_{OL} = 6mA
Fall time	t_F	-	-	TBD	ns	5V to 0.4V into 20pF
Capacitance	C_O	-	-	8	pF	including package
TP_RDP/TD_RDM differential output						
High level	V_H	1	-	3	V	
Zero level	V_0	-200	-	200	mV	
Low level	V_L	–1	-	–3	V	
Centred voltage	V_C	-	V_{DD}/2	-	V	

AC ELECTRICAL CHARACTERISTICS

Recommended operating conditions apply except where stated.

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Conditions
REFCLK						
Frequency			25±100ppm		MHz	
Duty cycle		45	-	55	%	
TXC						
10BASE-T Mode						
Frequency			20±100ppm		MHz	
Duty cycle		45	-	55	%	
100BASE-TX Mode						
Frequency			25±100ppm		MHz	
Duty cycle		45	-	55	%	
LOW-POWER Mode with RDOE=1						
Frequency			25±100ppm		MHz	
Duty cycle		40	-	60	%	
During transitions between modes						
High pulse width	t_{hi}	15	-	30	ns	for 1 cycle only
Low pulse width	t_{lo}	15	-	110	ns	for 1 cycle only
RXC						
10BASE-T Mode						
Frequency			20		MHz	
Duty cycle		45	-	55	%	during data reception
High pulse width		15	-	110	ns	during synchronization
Low pulse width		15	-	110	ns	during synchronization
100BASE-TX Mode						
Frequency			25		MHz	
Duty cycle		45	-	55	%	
During transitions between modes						
High pulse width	t_{hi}	15	-	30	ns	for 1 cycle only
Low pulse width	t_{lo}	15	-	110	ns	for 1 cycle only
TDAT[4:0] (100BASE-TX Mode only)						
Setup to TXC↑		-	-	20	ns	NIC applications
Hold from TXC↑		-	-	0	ns	NIC applications
Setup to REFCLK↑		-	-	10	ns	Repeater applications
Hold from REFCLK↑		-	-	0	ns	Repeater applications
TP-TDP (10BASE-T Mode only)						
Setup to TXC↓		-	-	10	ns	
Hold from TXC↓		-	-	0	ns	
RDAT[4:0] & DAT10 & SDT10						
Prop delay from RXC↓		0	-	7	ns	
SDT100						
Prop delay from RXC↑		0	-	7	ns	
RESET_N						
Pulse width		100	-	-	ns	

AC Characteristics TXOP/TXON in 10BASE-T Mode

Parameter	Reference
The peak differential voltage on the TD circuit when terminated with a 100Ω resistive load shall be between 2.2V and 2.8V for all data sequences.	802.3 - 14.3.1.2.1
When driven by an all-ones Manchester-encoded signal, any harmonic measured on the TD circuit shall be at least 27dB below the fundamental.	802.3 - 14.3.1.2.1
The TX10 Transmitter shal provide equalisation such that the output waveform shall fall within the template shown in 802.3 Fig 14-9 for all data sequences.	802.3 - 14.3.1.2.1
The Start-of-Idle pulse shall conform to the template of 802.3 Fig 14-10	802.3 - 14.3.1.2.1
The Link Pulse shall conform to the template of 802.3 Fig 14-12.	802.3 - 14.3.1.2.1
The differential output impedance as measured on TD shall be such that any reflection shall be at least 15dB below the incident.	802.3 - 14.3.1.2.2
The transmitter shall add no more than 3.5ns jitter when TD drives into 100Ω through the twisted pair.	14.3.1.2.3 802.3 -
The transmitter shall add no more than 8ns jitter when TD drives into 100Ω.	802.3 - 14.3.1.2.3
The common-mode to differential-mode balance shall exceed 29-17log10 (f/10) dB over the frequency range 1-20MHz.	802.3 - 14.3.1.2.4
The common-mode output voltage shall not exceed 50mV peak.	802.3 - 14.3.1.2.5
Application of a common-mode 15V peak 10.1MHz sinusoid to the test circuit shall not change the differentail voltage by more than 100mV and will add no more than 1ns jitter.	802.3 - 14.3.1.2.6
Application of a short circuit to TD shall not damage the circuit.	802.3 - 14.3.1.2.7
The short circuit shall not exceed 300mA.	802.3 - 14.3.1.2.7
The transmitter shall withstand without damage a 1000V common-mode impulse.	802.3 - 14.3.1.2.7
There shall be no extraneous signals on TD during normal power-up and power-down.	802.3 - 14.3.2.3

AC Characteristics TXOP/TXON in 100BASE-TX Mode

Parameter	Reference
The differential output voltage shall be in the range 950mV to 1050mV.	TP-PMD 9.1.2.2
The differential overshoot shall not exceed 5%.	TP-PMD 9.1.3.
Overshoot transients must decay to within 1% of the steady state voltage within 8ns of the start of the differential signal transition.	TP-PMD 9.1.3.
The signal amplitude symmetry shall be in the range 98% to 102%.	TP-PMD 9.1.4.
The return loss shall be greater than 16dB from 2MHz to 30MHz.	TP-PMD 9.1.5.
The return loss shall be greater than (16-20log (f/30MHz) dB from 30MHz to 60MHz.	TP-PMD 9.1.5.
The return loss shall be greater than 10dB from 60MHz to 80MHz.	TP-PMD 9.1.5.

AC Characteristics TXOP/TXON in 100BASE-TX Mode (Continued)

Parameter	Reference
The rise and fall times measured from 10% to 90% of the steady state output voltage shall be between 3ns and 5ns.	TP-PMD 9.1.6.
Difference between max. and min. rise and fall times shall be less than 0.5ns.	TP-PMD 9.1.6.
Duty cycle distortion must be less than ±0.25ns measured at 50% of the steady state output voltage for a data sequence of 01010101 (NRZ).	TP-PMD 9.1.8.
Total transmit jitter, including duty cycle distortionand baseline wander, must be less than 1.4ns peak to peak.	TP-PMD 9.1.9.

AC Characteristics RXIP/RXIN in 10BASE-T Mode

Parameter	Reference
Differential signals received on the RD that are within the envelope of 802.3 Figs 14-16 &14-17 shall be passed to RX10DATA.	802.3 14.3.1.3.1
RD signals with up to ±13.5ns zero crossing jitter is accepted.	802.3 14.3.1.3.1
RD signals corresponding to the envelope of 802.3 Fig 14-12 shall be accepted as a link pulse.	802.3 14.3.1.3.2
The receiver shall reject as data signals which would produce a peak magnitude of less than 300mV after being filtered through a 3-pole low-pass Butterworth with a 3dB cutoff at 15MHz.	802.3 14.3.1.3.2
The receiver shall reject as data continuous sinusoidal signals of amplitude less than 6.2V peak-to-peak and frequency less than 2MHz.	802.3 14.3.1.3.2
The receiver shall reject as data sine waves of single cycle duration,starting with phase 0 or 180 degrees, and of amplitude less than 6.2V peak-to-peak where the frequency is between 2MHz & 15MHz.	802.3 14.3.1.3.2
The RD circuit differential input impedance shall be such that the reflection of any signal in the frequency range 5MHz to 10MHz is at least 15dB below the incident.	802.3 14.3.1.3.4
The RD circuit common mode rejection shall be as defined in 802.3 14.3.1.3.5.	802.3 14.3.1.3.5
The RD circuit shall tolerate an indefinite short circuit.	802.3 14.3.1.3.6
The RD circuit shall withstand a 1000V common modeimpulse.	802.3 14.3.1.3.6

AC Characteristics RXIP/RXIN in 100BASE-TX Mode

Parameter	Reference
The return loss shall be greater than 16dB from 2MHz to 30MHz.	TP-PMD 9.2.2
The return loss shall be greater than (16dB-20 log(f/30MHz)) dB from 30MHz to 60MHz.	TP-PMD 9.2.2
The return loss shall be greater than 10dB from 60MHz to 80MHz.	TP-PMD 9.2.2

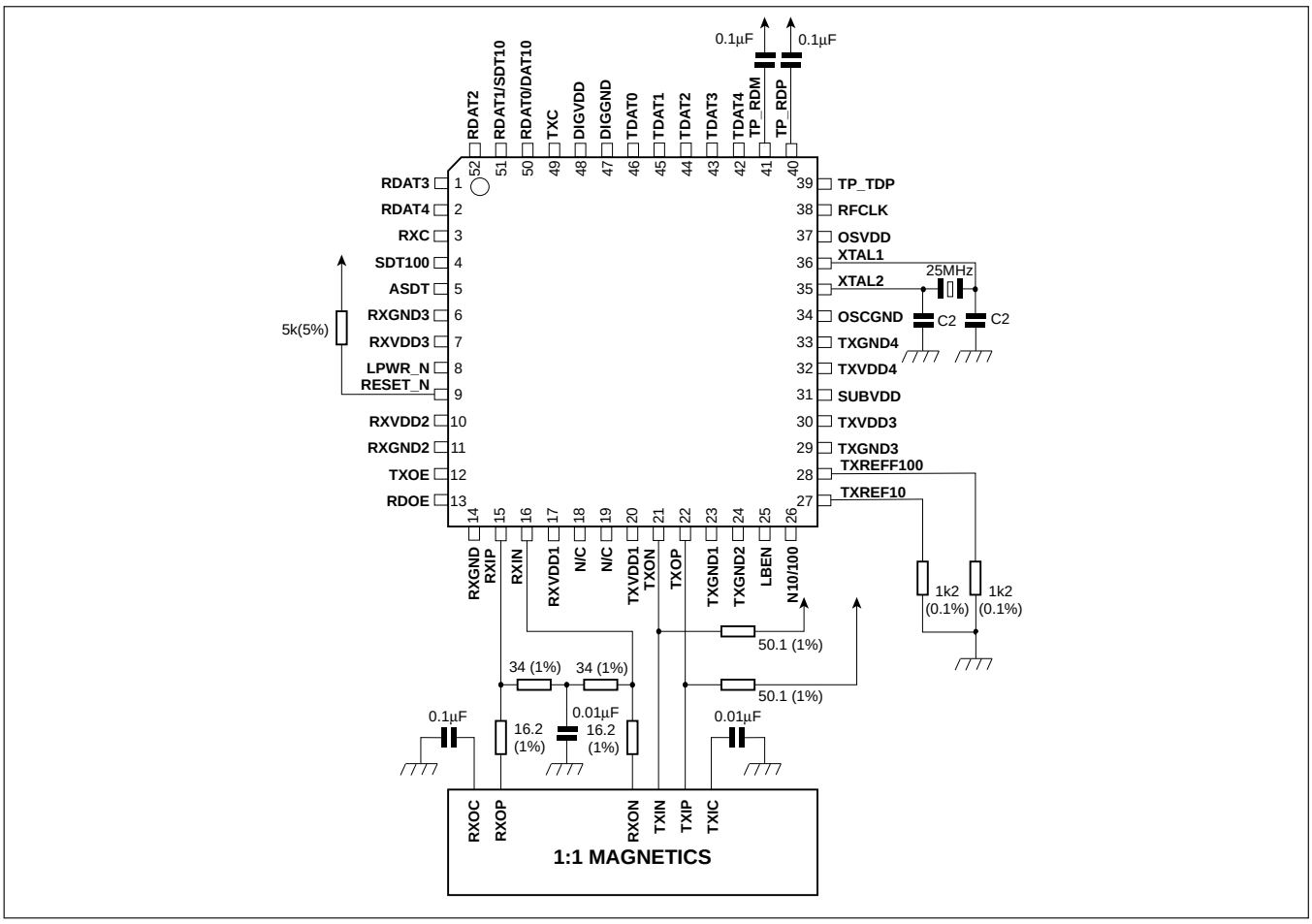


Fig.14 External components

EXTERNAL COMPONENTS

Connecting an External 25MHz Reference

If an external clock is used then it should be driven into the REFCLK input, and XTAL1 must be connected to OSCVDD. XTAL2 must be left unconnected.

RESET_N Pull-up Resistor

This resistor is required regardless of whether RESET_N is used externally.

TP-RDP/TP-RDM AC-coupling

TP-RDP/TP-RDM must be AC-coupled when working with a DEC21143 controller (or equivalent), but should be left unconnected when working with the NWK936.

RX Input Decoupling

The method of using a split input load resistor and de-coupling the centre tap reduces common mode noise.

Crystal Oscillator

For IEEE802.3 compliance the oscillator must run at 25MHz ±100ppm. The NWK939 on-chip circuitry contributes less than 40ppm variability to the oscillator frequency, therefore the crystal must be specified to 60ppm. This must include variations due to temperature and ageing.

External capacitors are required on the XTAL1 & XTAL2 pins. The values of these capacitors are dependent on the power dissipation and the equivalent series resistance of the chosen crystal, as follows:

Let P_C = power dissipation of the crystal in mW,

and ESR = equivalent series resistance of the crystal in W.

If P_C>2.6mW then C_1 & C_2 are determined by the loop gain:

$$C_1 = C_2 = \frac{184}{\sqrt{ESR}} \quad -7\text{pF}$$

If P_C<2.6mW then C_1 & C_2 are determined by the power dissipation of the crystal:

$$C_1 = C_2 = 114\sqrt{\frac{P_C}{ESR}} \quad -7\text{pF}$$

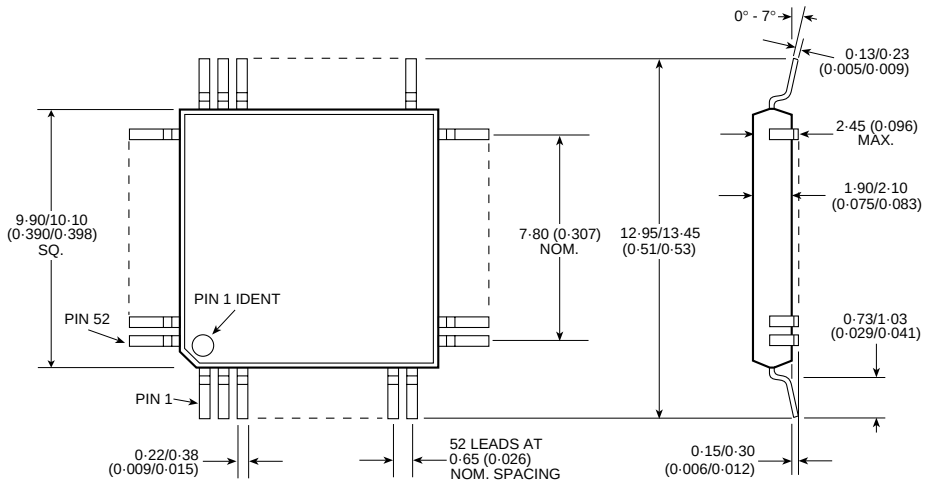
Tracking to the crystal and the capacitors must be as short as possible. Other signal paths must not cross the area.

The NWK939 is supported by magnetics from the following vendors:

VENDOR	MAGNETICS
Bel Pulse Valor	S558-5999-39 H1012 ST6118

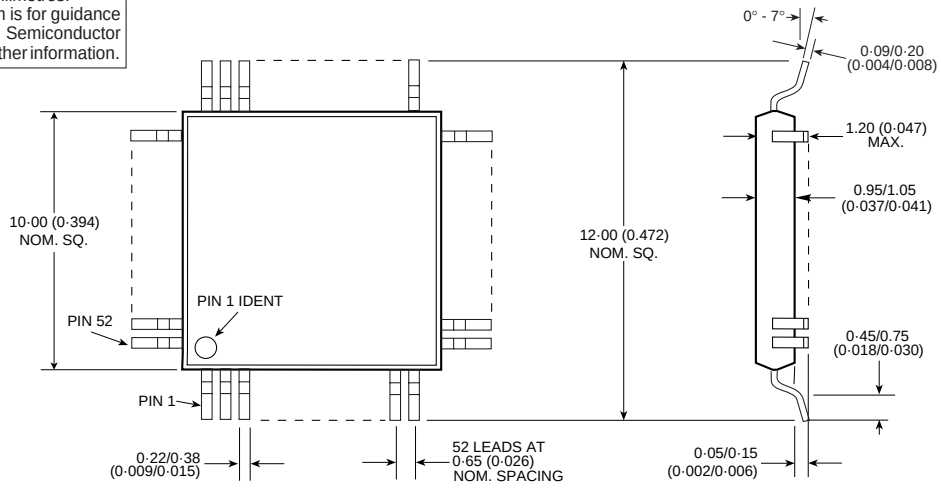
PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.



52-LEAD QUAD FLATPACK – GP52 (10 x 10 x 2.0mm)

NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your Mitel Semiconductor Customer Service Centre for further information.



52-LEAD THIN QUAD PLASTIC FLATPACK – TP52 (10 x 10 x 1.0mm)

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